Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. - 16. (Canceled)

17. (Currently Amended) A silicon-oxide-nitride-oxide-silicon structure comprising:

a first oxide layer arranged upon a silicon-based semiconductor substrate, wherein an interface between the silicon-based semiconductor substrate and the first oxide layer comprises deuterium;

a nitride layer arranged upon and in contact with the first oxide layer;

a second oxide layer arranged upon and in contact with the nitride layer; and

a second silicon layer arranged upon and in contact with the second oxide layer, wherein an interface between the second silicon layer and second oxide layer comprises deuterium.

18. (Original) The silicon-oxide-nitride-oxide-silicon structure of claim 17, wherein a lateral length of the interface between the silicon-based semiconductor substrate and the first oxide layer is bound by opposing sidewalls of the structure, and wherein said deuterium is arranged across an entirety of said lateral length.

19. (Canceled)

20. (Currently Amended) The silicon-oxide-nitride-oxide-silicon structure of claim ~~19~~17, wherein said nitride layer comprises deuterium.

21. (New) The silicon-oxide-nitride-oxide-silicon structure of claim 17, wherein an interface between the first oxide layer and the nitride layer comprises deuterium.

22. (New) The silicon-oxide-nitride-oxide-silicon structure of claim 17, wherein an interface between the nitride layer and the second oxide layer comprises deuterium.

23. (New) A semiconductor topography, comprising:

a silicon-oxide-nitride-oxide-silicon (SONOS) structure; and

a nitride layer comprising deuterium arranged above the SONOS structure.

24. (New) The semiconductor topography of claim 23, further comprising a dielectric layer comprising deuterium arranged above the nitride layer.

25. (New) The semiconductor topography of claim 23, wherein the SONOS structure comprises an oxide layer arranged upon and in contact with a silicon-based semiconductor substrate, wherein an interface between the silicon-based semiconductor substrate and the oxide layer comprises deuterium.

26. (New) The semiconductor topography of claim 23, wherein the SONOS structure comprises a deuiereated nitride layer.

27. (New) The semiconductor topography of claim 23, wherein the SONOS structure comprises a

an oxide layer; and

a silicon layer arranged upon and in contact with the oxide layer, wherein an interface between the silicon layer and the oxide layer comprises deuterium.

28. (New) The semiconductor topography of claim 23, wherein all layers of the SONOS structure comprise deuterium.

29. (New) The semiconductor topography of claim 23, wherein at least one but less than all the layers of the SONOS structure comprise deuterium.

30. (New) The semiconductor topography of claim 23, further comprising deutereated dielectric spacers interposed between the sidewalls of the SONOS structure and the nitride layer.

31. (New) A semiconductor topography comprising an oxide-nitride-oxide (ONO) structure, wherein at least one but less than all the layers of the ONO structure comprise deuterium.

32. (New) The semiconductor topography of claim 31, wherein at least one but less than all of the interfaces between the layers of the ONO structure comprises deuterium.

33. (New) The semiconductor topography of claim 31, further comprising a silicon-based semiconductor substrate upon which the ONO structure is arranged, wherein an interface between the silicon-based semiconductor substrate and a lower oxide layer of the ONO structure comprises deuterium.

34. (New) The semiconductor topography of claim 31, wherein the ONO structure comprises a deutereated nitride layer.

35. (New) The semiconductor topography of claim 31, further comprising a silicon layer arranged upon and in contact with the ONO structure, wherein an interface between the silicon layer and an upper oxide layer of the ONO structure comprises deuterium.

36. (New) The semiconductor topography of claim 31, further comprising a nitride layer comprising deuterium arranged above the ONO structure.

37. (New) The semiconductor topography of claim 36, further comprising a dielectric layer comprising deuterium arranged above the nitride layer.